

### **REMARKS/ARGUMENTS**

This case has been carefully reviewed and analyzed in view of the final Office Action dated 20 February 2008 and the preceding non-final Office Action dated 3 October 2007. Claims 1-23 remain pending herein.

In the final Office Action, the Examiner maintained his earlier rejection of Claims 1-23 under 35 U.S.C. 102(b) as being anticipated by the Lowe, et al. reference.

Before discussing the reference, it is believed beneficial to initially and briefly review the invention of the subject Patent Application. The subject Patent Application is directed to a method and system for automatic test generation comprising among its combination of features: automatically generating at least one test for testing a simulation model of a device under test (DUT) in a test environment during a test verification process by providing a plurality of scenarios, each scenario featuring at least one constraint relating to a relationship with at least one other scenario; selecting at least one scenario according to the at least one constraint by resolving conflicts among the constraints of the plurality of scenarios; and automatically generating the test from the at least one selected scenario to provide at least one input for driving simulated operation of the DUT.

In making the initial rejection, the Examiner correlated the compiling step of Lowe (Fig. 8 & Col. 20, ll 2-15) with the providing a plurality of scenarios, each scenario featuring at least one constraint relating to a relationship with at

least one other scenario. However, it is respectfully submitted that Lowe does not disclose, nor could a fair reading of Lowe suggest this limitation. Compiling is defined and known to one of skill in the art as the mere "translation of a higher level language program into machine language."

While compiling may connote some front end preprocessing, it is the compiler itself that maintains error checking rules and knowledge of limitations and not the source code. It is submitted that even were the scenarios correlated with the high level language source code, *arguendo*, the high level language source code does not feature constraints relating to relationships with others.

Thus, among many other distinctions, Lowe does not suggest, allude, or provide: "providing a plurality of scenarios, each scenario featuring at least one constraint relating to a relationship with at least one other scenario," as is necessary to independent Claim 1.

Alternatively, if the Examiner is seeking to correlate the VHDL models with the plurality of scenarios, this correlation must similarly fail. In Claim 1 of the subject Patent Application, it is made express that "generating the test from said at least one selected scenario to provide at least one **input** for driving the simulated operation of the DUT." In other words, the **scenarios will provide input to the Device Under Test (DUT)**. The VHDL models of Lowe: "e.g. microprocessors, memories, I/O devices etc..." more appropriately represent the actual device under test (DUT) and NOT the input or scenarios thereto. This is

clearly evinced in Lowe: "[t]his allows the VHDL model of the device under test to respond to the test stimulus ...." Therefore, the VHDL model can be a model of the DUT while the stimulus is more akin to an input. However, Lowe nowhere suggests or provides for the stimulus to have constraints relating to relationships with other stimulus.

The Examiner next correlated the resolving of data or bus cycles in Lowe (Col. 13, ll 4-13) with the step of: "selecting at least one of said plurality of scenarios according to said at least one constraint by resolving conflicts among said constraints of said plurality of scenarios...."

However, this correlation must also fail. The resolving of data or bus cycles as used in Lowe has a vastly different meaning from the "resolving of conflicts among constraints" as claimed in the subject Patent Application. The Examiner is urged to give the language of the claims their broadest reasonable meaning in light of the specification as MPEP 2111 mandates.

Lowe equates the word resolved with finished, as such: "...verifies that each byte of its transaction is accounted for and has been routed to the proper destination (step 130). In other words, a bus cycle state machine object remains in the TARGPEN state until it is **resolved** ...." (Col. 7, ll 42-50). Lowe bolsters this meaning with: "...resolved (i.e. clears the byte enable bit)." (Col. 12, line 44).

Lowe indeed contemplates and teaches that the resolving is the penultimate step rather than preparation for testing as in the subject Patent Application.

"When **all resolution checks are completed** in the TARGPEN state 128 the state machine object transitions to the **FINISH** state illustrated by step 132 which signals that the bus cycle is complete and the state machine object can be destroyed." (Col. 7, ll 50-60); and "...having been completely resolved, thus enters into its FINISH state 132 (Fig. 5C) indicating cycle completion..." (Col. 13, ll 10-13).

Whereas, in the subject Patent Application, the "**selecting** at least one of said plurality of **scenarios according to said at least one constraint by resolving conflicts among said constraints** of said plurality of scenarios" is performed well in advance of test completion. Indeed, the test has not even been generated or run yet when resolving conflicts among constraints in the subject Patent Application.

Therefore, the use of "resolved" in Lowe to merely signal conclusion of the tests must be understood by one of ordinary skill in the art to be vastly disparate from the "resolving of constraints" as claimed in the subject Patent Application. It cannot be fairly said that Lowe anticipates this step of the subject Patent Application merely because it happens to use the same word, especially when the same word has completely different meanings as applied to completely different steps.

Still further, there is no where suggested that the stimulus in Lowe could conflict, no teaching of constraints being featured in the stimulus. There is not

even a teaching or suggestion that constraints could relate to relationships among scenarios.

Thus, Lowe does not suggest or provide, and indeed teaches away from the provision of: "selecting at least one of said plurality of scenarios according to said at least one constraint by resolving conflicts among said constraints of said plurality of scenarios," as is necessary to independent Claim 1.

It is respectfully submitted, therefore, that the cited Lowe, et al. reference fails to disclose the unique concatenation of interrelated steps recited by the pending Claims for the purposes and objectives disclosed in the subject Patent Application.

Given the deficient and contrary teachings of the primarily cited Lowe reference, the Examiner is respectfully requested to revoke the issued anticipation rejection.

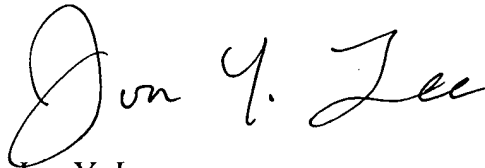
The dependent Claims are believed to show further patentable distinctions, but are believed allowable for at least the reasons presented supra.

It is now believed that the subject Patent Application has been placed fully in condition for allowance, and such action is respectfully requested.

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Reply to Office Action dated 20 February 2008

No fees are believed to be due with this Amendment. If there are any charges associated with this filing, the Honorable Commissioner for Patents is hereby authorized to charge Deposit Account #18-2011 for such charges.

Respectfully submitted,  
For: ROSENBERG, KLEIN & LEE

A handwritten signature in black ink, appearing to read "Jun Y. Lee". The signature is fluid and cursive, with the first name "Jun" and last name "Lee" being more prominent than the middle initial "Y".

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